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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,339	04/18/2001	Takahiro Fujioka	HITA.0048	8737

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REED SMITH LLP
3110 FAIRVIEW PARK DRIVE, SUITE 1400
FALLS CHURCH, VA 22042

EXAMINER	
KUMAR, SRILAKSHMI K	

ART UNIT	PAPER NUMBER
2675	11

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,339	FUJIOKA ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to Amendment C, filed, February 17, 2004. Claims 1 and 5 have been amended. Claims 1-15 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya et al (US 5,091,784) in view of Murata et al (US 6,144,355), further, in view of Sasaki et al (US 6,211,849) and further, in view of Shibata et al. (US 5,754,838).

As to independent claims 1 and 5, Someya et al disclose a liquid crystal display device having a liquid crystal display panel, a plurality of cascade-connected and liquid crystal drive circuits for sequentially transferring a signal (Fig. 2), and a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits (Fig. 2), wherein each of the liquid crystal drive circuits comprises; an image input terminal connected with one of the signal lines to receive an image signal being input thereto (col. 5, lines 30-59); a clock input terminal connected with another one of the signal lines to receive an external clock signal being input thereto (input into Fig. 2, item 8, clock generator); a clock compensation circuit (Fig. 2, item 8, clock generator) for generating an internal clock based on the external clock signal by compensating for a duty ratio deviation from the external clock signal, said internal clock signal swinging from a first voltage to a second voltage lower

than the first voltage (col. 7, lines 41-52); the clock formation circuit being operable to correct the internal clock based on the external clock (col. 6, line 61-col. 7, lines 5, 41-52), Someya discloses in col. 6, line 61-col. 7, line 5, where based on input into the clock generator, different output clocks are generated. Murata et al discloses a clock compensation circuit for generating an internal clock based on the external clock signal by compensating for a duty ratio deviation from the external clock signal in col. 3, lines 42-60. It would have been obvious to one of ordinary skill in the art to incorporate the duty ratio deviation as is disclosed in col. 3, lines 42-60, as with such an arrangement, since the duty ratio of the clock signal being output to the signal line driver circuit is corrected to be approximately 50%, even where the operation speed is increased to attain high precision, accurate image data sampling can be accomplished enabling achievement of excellent display images with enhanced quality.

a data storage circuit for storing therein the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal (Fig. 2, item 25, col. 7, lines 41-52); a data bus for transmitting the image signal to be output from the data storage circuit (col. 10, lines 15-50), and a voltage select circuit for selecting a voltage for driving the liquid display panel (Fig. 15, item 107); and,

Someya et al and Murata et al do not disclose a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal to a subsequent liquid crystal drive circuit. Sasaki et al disclose in Figs. 4 and 5, a clock signal output circuit where the internal clock signal is output to a subsequent liquid crystal drive circuit as is also disclosed in col. 4, lines 46-67, col. 5, lines 5-12, 30-41. It would have been obvious to one of ordinary skill in the

art to incorporate this feature into that of Someya et al as with the clock signal output circuit enables a liquid crystal display device of achieving higher resolution by regulating the duty cycle ratio as disclosed in col. 2, lines 25-col. 3, lines 3.

Someya et al and Murata et al do not disclose wherein the clock signal output circuit has a delay circuit. Sasaki et al disclose a delay circuit, but do not disclose where the delay circuit delays the clock signal so as to provide phase margins there of in a dual edge accept scheme.

In a similar field of endeavor, Shibata et al disclose a system (col. 1, lines 25-27), which generates internal clock signals necessary for operating the synchronous DRAM circuit in an internal circuit utilizing a known PLL (phase locked loop) or DCC (delay locked loop) circuit. In col. 16, lines 58-67, Shibata et al disclose a DLL circuit comprising a phase comparator which compares external clock signals fed through an external terminal with internal clock signals, a loop filter which converts the output signals of the phase comparator into a direct current, a delay circuit for generating said internal clock signals having the same frequency as said external clock signals, but having delay relative to the external clock signals. It would have been obvious to incorporate the delay circuit of Shibata et al into that of Someya, Murata and Sasaki et al as disclosed in col. 1, lines 18-59, as operation speed would be improved.

As to dependent claims 2 and 6, limitations of claims 1 and 5, and further comprising, wherein the clock compensation circuit has a phase locked loop circuit (Fig. 31, item 121).

As to dependent claims 3 and 7, limitations of claims 1 and 5, and further comprising, wherein the clock compensation circuit has a delay locked loop circuit. Although Someya et al do not disclose the delay locked loop circuit, it would have been obvious to one of ordinary skill

in the art to incorporate this feature as the delay locked loop circuit is advantageous as it allows for phase shift as opposed to no shifting.

As to dependent claims 4 and 8, limitations of claims 1 and 5, and further comprising, wherein the data bus comprises two systems of signal lines (Fig. 2, input from sample-hold circuit and terminal 29).

As to dependent claims 9 and 11, limitations of claims 1 and 5, and further comprising, wherein the duty ratio deviation of the external clock signal is caused by at least one of an internal characteristic of the respective drive circuit and a factor on the signal lines. Someya et al do not disclose the feature of the duty ratio deviation caused by at least one of an internal characteristic. Murata et al discloses a duty ratio deviation from the external clock signal is caused by at least one of an internal characteristic of the respective drive circuit and a factor on the signal lines in col. 3, lines 42-60. It would have been obvious to one of ordinary skill in the art to incorporate the duty ratio deviation as is disclosed in col. 3, lines 42-60, as with such an arrangement, since the duty ratio of the clock signal being output to the signal line driver circuit is corrected to be approximately 50%, even where the operation speed is increased to attain high precision, accurate image data sampling can be accomplished enabling achievement of excellent display images with enhanced quality.

As to dependent claims 10 and 12, limitations of claims 1 and 5, and further comprising, wherein the internal clock signal generated by the clock compensation circuit has a duty ratio of 50%. Someya et al do not disclose a duty ratio of 50%. Murata et al discloses a duty ratio of 50% in col. 3, lines 42-60. It would have been obvious to one of ordinary skill in the art to incorporate the duty ratio deviation as is disclosed in col. 3, lines 42-60, as with such an

arrangement, since the duty ratio of the clock signal being output to the signal line driver circuit is corrected to be approximately 50%, even where the operation speed is increased to attain high precision, accurate image data sampling can be accomplished enabling achievement of excellent display images with enhanced quality.

As to dependent claims 13 and 14, limitations of claims 1 and 5, and further comprising, wherein the clock compensation circuit has an inverter. Someya et al do not disclose a clock compensation circuit with an inverter. Murata et al discloses a clock compensation circuit for generating an internal clock based on the external clock signal by compensating for a duty ratio deviation from the external clock signal in col. 3, lines 42-60. Murata et al disclose where the clock compensation circuit has an inverter in col. 5, lines 41-67, Fig. 1, items 9 and 56. It would have been obvious to one of ordinary skill in the art to incorporate the duty ratio deviation as is disclosed in col. 3, lines 42-60, as with such an arrangement, since the duty ratio of the clock signal being output to the signal line driver circuit is corrected to be approximately 50%, even where the operation speed is increased to attain high precision, accurate image data sampling can be accomplished enabling achievement of excellent display images with enhanced quality.

As to dependent claim 15, limitations of claim 1, and further comprising, wherein the voltage select circuit selects the voltage according to the image signal on the data bus and then outputting the selected voltage (Fig. 15, item 107, col. 13, lines 11-18).

Response to Arguments

3. Applicant's arguments with respect to claims 1 and 5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 703 306 5575. The examiner can normally be reached on 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, xxxx xxxx can be reached on xxx xxx xxxx. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 4700.

Srilakshmi K. Kumar
Examiner
Art Unit 2675

SKK
May 12, 2004

DENNIS-DOON CHOW
PRIMARY EXAMINER